

CLAIMS

What is claimed is:

1 1. A semiconductor device comprising:
2 a charge pump circuit comprising a plurality of charge pump cascades, each
3 of the charge pump cascades comprising a plurality of pump stages; and
4 wherein the plurality of charge pump cascades are driven to pump charge
5 to a common output in response to alternate edges of a system clock signal.

1 2. The semiconductor device of claim 1, further comprising a non-
2 overlapping clock signal generator, the non-overlapping clock signal generator
3 generating non-overlapping clock signals in response to alternate rising and falling
4 edges of the system clock signal.

1 3. The semiconductor device of claim 1, wherein the common output
2 provides an output supply voltage that is greater than a power supply voltage
3 provided to the charge pump circuit.

1 4. A memory device including a charge pump circuit comprising:
2 a first and second charge pump cascade, the first and second charge pump
3 cascade comprising a plurality of charge pump stages;
4 each of the plurality of charge pump stages comprising a transistor and a
5 capacitor; and
6 wherein the plurality of charge pump stages pump charge to an output node
7 on both a rising edge and a falling edge of a system clock signal.

1 5. The memory device of claim 4, wherein the transistor comprises a
2 PFET configured as a diode.

1 6. The memory device of claim 4, wherein the capacitor comprises a
2 PFET configured as a capacitor.

1 7. The memory device of claim 4, wherein the first and second charge
2 pump cascades receive a power supply voltage and are in communication with the
3 output node and wherein the output node provides an output supply voltage that is
4 greater than the power supply voltage.

1 8. The memory device of claim 4, further comprising a non-
2 overlapping clock signal generator for generating a first and a second phase signal
3 in response to opposite phases of the system clock signal wherein the first phase
4 signal drives (2n)th charge pump stage of the first charge pump cascade and (2n
5 +1)th charge pump stage of the second charge pump cascade and wherein the
6 second phase signal drives (2n + 1)th charge pump stage of the first charge pump
7 cascade and (2n)th charge pump stage of the second charge pump cascade, n being
8 an integer greater than or equal to zero.

1 9. A charge pump comprising:
2 a first and a second pump cascade coupled in parallel to an output node;
3 the first and the second pump cascades comprising a plurality of pump
4 stages coupled in series;
5 wherein (2n)th pump stage of the first pump cascade is coupled to receive
6 a first clock signal and (2n+1)th pump stage of the first pump cascade is coupled
7 to receive a second clock signal, n being an integer greater than or equal to zero;
8 wherein (2n)th pump stage of the second pump cascade is coupled to
9 receive the second clock signal and (2n + 1)th pump stage of the second pump

10 cascade is coupled to receive the first clock signal, n being an integer greater than
11 or equal to zero; and
12 wherein the output node receives charge pumped by the first and the second
13 pump cascades and provides an output supply voltage that is greater in magnitude
14 than the power supply voltage.

1 10. The charge pump of claim 9, wherein each pump stage comprises
2 a PFET configured as a diode and a PFET configured as a capacitor.

1 11. The charge pump of claim 9, wherein a first pump stage of each of
2 the first and second pump cascades comprises a thin oxide PFET configured as a
3 diode and a thin oxide PFET configured as a capacitor.

1 12. A charge pump for generating a high voltage supply comprising:
2 a first pump cascade comprising multiple charge pump stages, each charge
3 pump stage in the first pump cascade being driven by a first plurality of clock
4 signals;

5 a second pump cascade comprising multiple charge pumps stages, each
6 charge pump stage in the second pump cascade being driving by a second plurality
7 of clock signals;

8 a non-overlapping clock signal generator for generating the first and second
9 plurality of clock signals in response to transitions in a system clock signal, each

10 of the clock signals of the second plurality of clock signals having opposite phases
11 to each of the clock signals of the first plurality of clock signals; and
12 wherein final charge pump stages of the first and second pump cascades are
13 coupled in parallel to provide the high voltage supply.

1 13. A memory device including a charge pump comprising:
2 a first and second charge pump cascade, the first and second charge pump
3 cascade comprising a plurality of charge pump stages;
4 wherein each of the plurality of charge pump stages comprises a means for
5 receiving charge and a means for storing charge; and
6 means for driving an output node with charge stored in the plurality of
7 charge pump stages on both a rising edge and a falling edge of a system clock
8 signal.

1 14. The memory device of claim 13, wherein the means for receiving
2 charge comprises a PFET configured as a diode.

1 15. The memory device of claim 13, wherein the means for storing
2 charge comprises a PFET configured as a capacitor.

1 16. The memory device of claim 13, wherein the first and second charge
2 pump cascades are powered by a power supply voltage and are coupled in common
3 to the output node and wherein the output node provides an output supply voltage
4 that is greater than the power supply voltage.

1 17. The memory device of claim 13, wherein means for driving an
2 output node comprises a first and a second phase signal comprising opposite phases
3 of the system clock signal wherein the first phase signal drives (2n)th charge pump
4 stage of the first charge pump cascade and (2n +1)th charge pump stage of the
5 second charge pump cascade and wherein the second phase signal drives (2n +
6 1)th charge pump stage of the first charge pump cascade and (2n)th charge pump
7 stage of the second charge pump cascade, n being an integer greater than or equal
8 to zero.

1 18. A method for generating a voltage greater than a power supply
2 voltage, comprising the steps of:
3 providing the power supply voltage to a plurality of pump cascades
4 comprising a plurality of pump stages;

5 on a first edge of a system clock, storing charge from a power supply
6 simultaneously in a first group of charge pump stages and pumping charge to an
7 output node from a second group of charge pump stages; and
8 on a second edge of the system clock, storing charge from the power supply
9 simultaneously in the second group of charge pump stages and pumping charge to
10 the output node from the first group of charge pump stages.

1 19. A method of operating a plurality of charge pump cascades, each
2 charge pump cascades comprising a first and second group of charge pump stages,
3 and wherein the charge pump cascades operate to pump electrical charge to an
4 output supply node, the method comprising the steps of:
5 in response to a leading edge of a system clock, pre-charging output nodes
6 of the first group of charge pump stages to voltages present on respective input
7 nodes in the first group of charge pump stages and subsequently boosting output
8 nodes of the second group of charge pump stages to respective boosted voltages;
9 in response to a trailing edge of the system clock, pre-charging output nodes
10 in the second group of charge pump stages to voltages present on respective input
11 nodes in the second group of charge pump stages and subsequently boosting output
12 nodes in the first group of charge pump stages to respective boosted voltages; and

13 providing charge in alteration from each of the charge pump cascades to the
14 output supply node in response to both leading and trailing edges of the system
15 clock until the output supply node reaches a predetermined voltage level.

1 20. A non-overlapping clock signal generator comprising:
2 a system clock input node;
3 a clock input stage;
4 a latch coupled to the clock input stage having intermediate latch outputs
5 and complementary latch outputs;
6 clock output driving stages coupled to the complementary latch outputs and
7 having non-overlapping clock signal outputs; and
8 and equalization stage coupled between the clock output driving stages and
9 receiving as inputs the intermediate latch outputs.